

SAX248

[30 – 88] MHz Tunable Bandpass Filter

Application

The SAX248 electronically tunable bandpass filter is designed for Tactical Communications Applications using binary weighted digital tunable capacitor arrays to cover greater than an octave bandwidth.

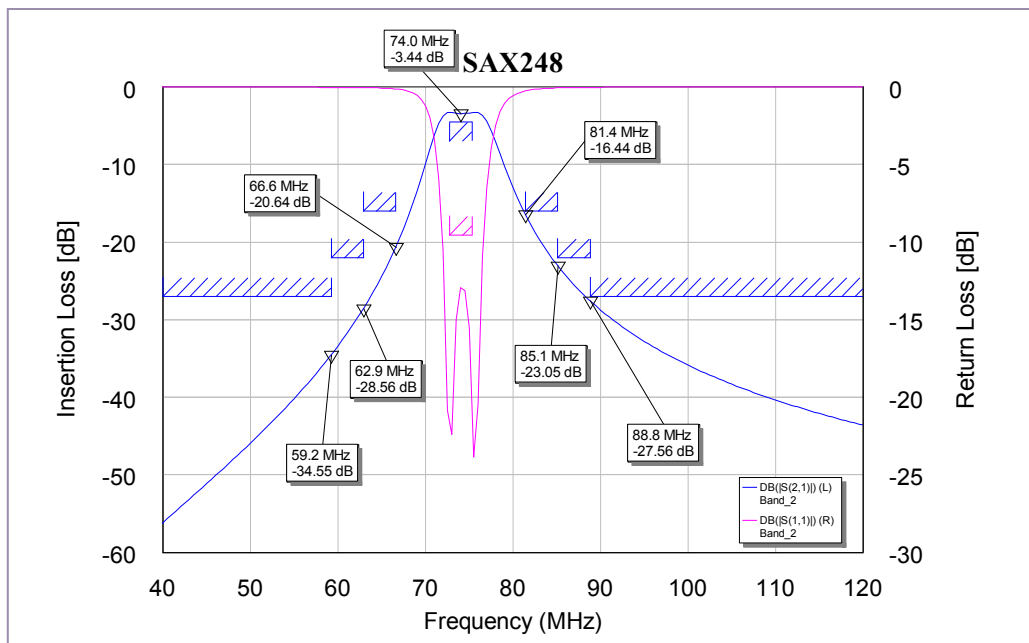
Features

- Full Tactical Communications band resolutions
- Low insertion loss
- Fast tuning across band to 0.5 MHz resolution
- 33 dBm P1dB
- DC power < 70 mW



Specifications

Mechanical	Dimensions	1.2 x 0.65 x 0.25 inches
RF Power Handling	IIP3	+45 dBm
	P1dB	+33 dBm
Filter Performance	Tuning Range	[30 – 88] MHz
	Input / Output Impedance	50 ohm
	Tuning Step Size	0.5 MHz
	Bandpass Bandwidth	3.5% typical, 5% max.
	Insertion Loss @ fc	< 4.5 dB
	Bandpass VSWR	1.5:1 typical, 2.0:1 max.
	Rejection	Ftune +/- 10% > 15 dB typical Ftune +/- 15% > 20 dB 10 MHz to 0.5*Ftune > 40 dB [2*Ftune to 500] MHz > 35 dB
Control & Interface	Tuning Control	Serial [SPI]
	DC Power	<80 mW
	Tuning Speed	= 35 μs
	Tuning Algorithm	Tuning Word = (Ftune - 30)/0.5



SPI Communication Interface

The SAX248 Tunable Filter is controlled as a slave SPI device.

The control registers are write only so there are only three SPI signals required:

- CS input: when low, the SPI bus is enabled. When high, signals on the other SPI inputs are ignored.
- SCLK: serial data clock generated by the SPI bus master.
- MOSI: data from master to slave (Master Out, Slave In).

The timing of the SPI bus is:

- The base value of the clock is low (0).
- The SAX248 reads the incoming data (MOSI) on the rising edge of the clock SCLK.
- The maximum allowed SCLK rate is 1.0 MHz.

A single 8-bit tuning byte is transmitted to the filter. The filter will begin to tune to the new frequency upon receipt of the last of the 8 bits. The valid range of tuning bytes in this mode is 0x00 to 0xFA (0 to 250 decimal).

The figure below shows the SPI bus set command operation:

- The SPI bus master sets CS low and generates the SCLK.
- The master sends an 8-bit filter select word (MSB first) on the MOSI line.
- After the last clock pulse, the SPI bus master sets CS high.

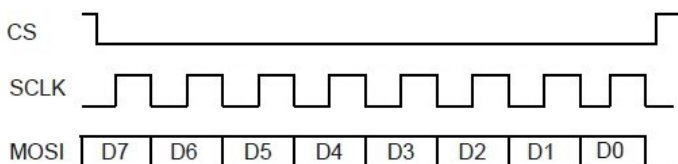
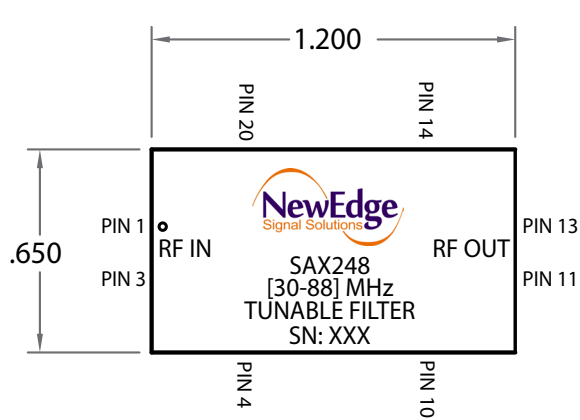
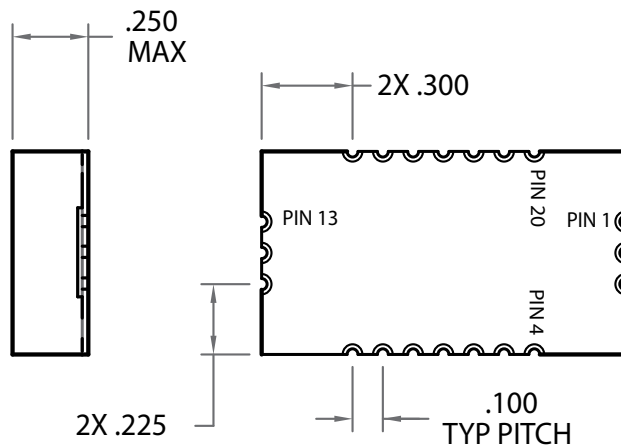


Figure 1 – SAX248 Mode One SPI Control Interface

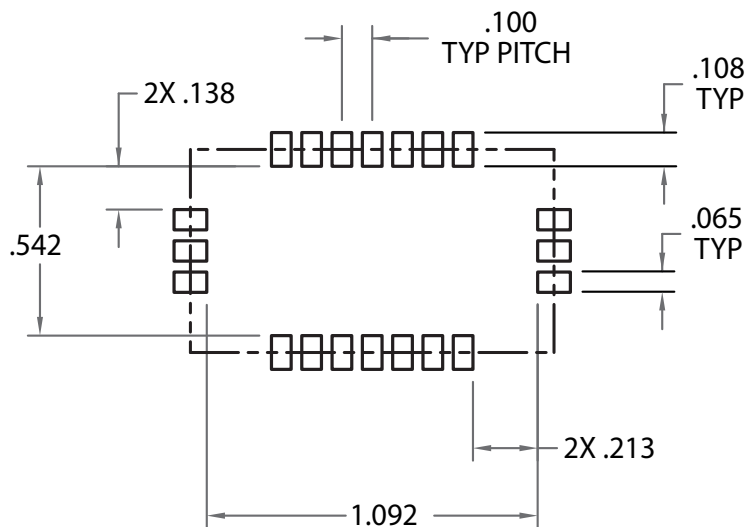


(TOP VIEW)



(BOTTOM VIEW)

RECOMMENDED LAND PATTERN



Pin	Description
1	GROUND
2	RF IN
3	GROUND
4	GROUND
5	ICSPCLK
6	ICSPDAT
7	MCLR
8	GROUND
9	TEMP
10	GROUND
11	GROUND
12	RF OUT
13	GROUND
14	GROUND
15	VCC +3.3V
16	GROUND
17	SPI CS
18	SPI MOSI
19	SPI CLK
20	GROUND

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